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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/921,471	08/03/2001	David Marshall	10014782-1	7017

7590 04/06/2004

HEWLETT-PACKARD COMPANY  
Intellectual Property Administration  
P.O. Box 272400  
Fort Collins, CO 80527-2400

EXAMINER

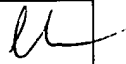
NGUYEN, MINH T

ART UNIT PAPER NUMBER

2816

DATE MAILED: 04/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 09/921,471	<b>Applicant(s)</b> MARSHALL ET AL. 	
	<b>Examiner</b> Minh Nguyen	<b>Art Unit</b> 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 12 January 2004.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 8-13 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 8-13 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 August 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>1/12/04</u> . | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. Applicant's amendment filed on 1/12/04 has been received and entered in the case.

Claims 8-13 are pending. New grounds or rejections necessitated by the amendment are set forth below. This action is FINAL.

#### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 4,574,206, issued to Todokoro et al.

As per claim 8, Todokoro discloses a method (Fig. 1) for receiving a digital signal (at node 10, Figs. 2A and 2B show the input is digital), comprising:

comparing (by the comparator 12, column 3, lines 23-24) the digital signal to a reference voltage (the voltage at node 16, column 3, lines 23-24);

determining when the digital signal has changed from greater than the reference voltage to less than the reference voltage (column 3, lines 28-29); and

reducing the reference voltage after the digital signal has changed from being greater than the reference voltage to being less than the reference voltage (column 3, lines 29-30) wherein the

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reference voltage is reduced by selecting different node (change the selection from node 18 to node 24), the reference voltages at nodes 18 and 24 are provided by two sources 20 and 22 connected as a ladder.

Todokoro does not explicitly teach the reference voltages at node 18 and 24 are provided by a resistive ladder as called for in the claim.

The examiner takes Official Notice the fact that using a resistive ladder for supplying various reference voltages to an input terminal of a comparator are old and well-known in the art. Such fact is notoriously well-known that it is even taught in electronic textbooks. In fact, many of the related references cited in previous Office actions used resistive ladder for providing reference voltages. For example, reference '834 teaches in Fig. 2 the use of resistive ladder for providing reference voltages to an input of a comparator, reference '329 teaches in Fig. 1 the use of resistive ladder for providing reference voltages to an input of a comparator. In practice, many power supplies providing variable reference voltages using potentiometers which are resistive ladders for providing variable voltages.

It would have been obvious to one skilled in the art at the time of the invention was made to replace the two voltage sources 20 and 22 in the Todokoro circuit by a resistive ladder. The motivation would be to reduce the number of the power sources needed to provide reference voltages for the Todokoro circuit.

As per claim 9, Todokoro discloses a method comprises steps recited as discussed in claim 8, he explicitly discloses the clock signal 28 (the waveform is shown in Fig. 2D) is used to control the timing of the reference voltage and the clock signal has the frequency higher than the frequency of input signal.

Todokoro does not explicitly disclose the clock signal has a frequency so that the reference voltage is reduced over a period of time that is greater than the expected time for the digital signal changes from one state to another, i.e., it is merely a matter of varying the frequency of the clock signal.

However, it has been ruled that “where the general conditions of a claim are disclosed in the prior art reference, it is not inventive to discover the optimum or workable ranges by routine experimentation.”. See MPEP 2144.05 for further discussions.

It would have been obvious to one skilled in the art at the time of the invention was made to adjust the frequency of the clock signal in the Todokoro circuit frequency so that the reference voltage is reduced over a period of time that is greater than the expected time for the digital signal changes from one state to another.

The motivation/suggestion for that would be to obtain a workable range for Tokodoro circuit in applications which call for such particular range.

As per claims 10-11, these claims are rejected for the same reasons and motivation noted in claims 9-10, respectively. The recited “increasing” on line 7 of claim 10 is taught in column 3, lines 30-31.

As per claim 12, Todokoro discloses a method (Fig. 1), comprising:

adjusting a reference between a first nominal reference level and a second nominal reference level (by switching the switch 14 from node 18 to node 24);

adjusting the reference between the second nominal reference level and the first nominal reference level (by switching the switch 14 from node 24 to node 18);

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comparing (using the comparator 12) signal (at node 10) to the first nominal reference level when the signal is closer to the first nominal reference level than the second nominal reference level (the description is on column 3, lines 21-34); and

comparing (using the comparator 12) the signal (at node 10) to the second nominal reference level when the signal is closer to the second nominal reference level than the first nominal reference level (also description is on column 3, lines 21-34).

Todokoro does not explicitly teach the reference voltages are provided by a resistive ladder as called for in the claim.

However, this missing limitation is seen as an obvious modification for the same reasons and motivations discussed in claim 8 herein above.

As per claim 13, the recited limitation is met because it is clear that the result of the comparison by the comparator 12 is used to initiate the counter 26 to adjust the reference levels (20 and 22) by the selector 14.

### ***Double Patenting***

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 8-13 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 16-19 of copending Application No. 10/447,929. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 8-13 in this instant application are merely the method to operate the apparatus of claims 16-19 in the copending Application No. 10/447,929. When the apparatus recited in claims 16-19 is disclosed, the method to operate such an apparatus is obviously seen by a person skilled in the art.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

#### ***Response to Arguments***

4. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

#### ***Conclusion***

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

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will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 571-272-1748. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



4/2/04

Minh Nguyen  
Primary Examiner  
Art Unit 2816